ARTEMIS: A 40 Gb/s All-Optical Self-Router using Asynchronous Bit and Packet-Level Optical Signal Processing

[1]*L. Stampoulidis,* [1]*E. Kehayas,* [1]*K. Vyrsokinos,* [2]*K. Christodoulopoulos,* [1]*D. Tsiokos,* [1]*P. Bakopoulos,*
[1]*G. T. Kanellos,* [2]*K. Vlachos,* [2]*E. A. Varvarigos and* [1]*H. Avramopoulos*

[1]Photonic Communication Research Laboratory, National Technical University of Athens

[2]Communication Networks Laboratory,
Research Academic Computer Technology Institute, University of Patras

Abstract— **We present a 40 Gb/s asynchronous self-routing network and node architecture that exploits bit and packet level optical signal processing to perform synchronization, forwarding and switching. Optical packets are self-routed on a hop-by-hop basis through the network by using stacked optical tags, each representing a specific optical node. Each tag contains control signals for configuring the switching matrix and forwarding each packet to the appropriate outgoing link and onto the next hop. Physical layer simulations are performed, modeling each optical sub-system of the node showing acceptable signal quality and Bit Error Rates. Resource reservation-based signaling algorithms are theoretically modeled for the control plane capable of providing high performance in terms of blocking probability and holding time.**

I. INTRODUCTION

The migration from current WDM networks employing circuit switching technology to optical packet switched networks (OPS) has been identified as a key issue, since the former can not provide bandwidth-on-demand and are not suitable for "greedy" applications involving bursty traffic. To draw this migration path, the attention has been focused on the identification of the functionalities required in a packet switched node and how these could be best carried out in the optical domain [1]. Signal conditioning, synchronization and routing have been identified as the main classes of operations that should be performed in order to be able to switch optical packets in a photonic network. The application of optical signal processing techniques to realize these applications has become feasible due to the development and commercialization of optical logic elements, such as optical gates and interferometric switches. These optical logic elements are suitable for high-speed signal processing and they have been established as the fundamental building blocks of all-optical switching nodes. In this context, all-optical gates have been used as core elements performing a diversity of functionalities, such as data regeneration, clock recovery, header/payload separation, header matching and data recovery [2].

Despite the above achievements, integration of functionalities in a system environment to perform lossless packet processing and routing in the optical domain still remains an elusive target. The routing plane is the most demanding in terms of intelligence required in the optical layer and the limitations imposed stem from the lack of optical RAM capable of storing information. Thus, the node local address generation procedure is difficult and does not scale well with increased number of header bits when implemented with fiber delay lines. In addition the look-up table cannot be implemented with current photonic technology, although revolutionary research has been reported [3] that could initiate an evolution path towards photonic RAM.

As optical buffers are far from practical and given the lack of an optical random access memory, there has been considerable attention towards the design and implementation of bufferless, self-routing switches to eliminate O/E/O conversions associated with packet address reading. In a self-routing network the intermediate nodes forward the incoming packets to the appropriate output ports according to information embedded at the source node. The case where the routing decisions are made on the basis of single-bit information in the header is also referred to as bit-level packet switching [4] and employs optical processing of the header. Although self-routing offers simple routing control in an OPS network node, its implementation imposes specific requirements concerning the operation of the optical logic circuits involved. For an all-optical self-routing node to operate, it is of vital importance to be able to generate the optical signals controlling the node gates in order to achieve routing on a packet by packet basis through the switching matrix. This implies that each packet should be handled as an independent entity and the control signals generated should persist only for the duration of each data packet. To address these issues self-routing techniques employing self-clocking [5], all-optical address recognition [4] and serial-to-parallel conversion label recognition [6] have been demonstrated. Self-clocking has been one of the standard techniques for self-routing of optical packets posing specific constraints for the

transmitters as it requires that each packet can carry its own clock. More recently, serial to parallel conversion schemes have been shown to route 40 Gb/s optical packets requiring, however, electronic memories and processing.

In this communication we propose and theoretically evaluate a self-routing network architecture, ARTEMIS, which is able to perform successfully without the intervention of electronics and avoids the need for optical header recognition and decoding at each node, using simple all-optical circuits. The primary goal of ARTEMIS is to achieve packet switching with bit-level processing, exploiting the performance of optical gates at high data rates. All the routing decisions are performed on-the-fly using information embedded in the header, thus avoiding O/E/O conversions or local address generation and all-optical header recognition. The switch inherently operates on a packet-by-packet basis and is capable of routing 40 Gb/s asynchronous packets, adding flexibility and true transparency to the network. In addition, the switch is self-synchronizing and thus does not require phase synchronization with local electrical or optical oscillators. When combined with appropriate control protocols the proposed switch architecture can provide packet-mode communication and potentially eliminate the data bottlenecks at the routing controller avoiding the time consuming search and updating of look up tables.

II. ARTEMIS NETWORK ARCHITECTURE

A. Self-Routing Concept

The self-routing network architecture proposed is shown in Fig. 1 and consists of two clearly defined layers. All network functionalities associated with transmission, regeneration and routing are performed in the optical layer. The electrical control plane is responsible for resources reservation and connection establishment. The transmission of optical packets is realized using optical headers that contain stacked optical "tags", each corresponding to a specific node. Hence, optical tag contains bit-level information for optically controlling the switching matrix of the node and thus routing the data packet to the appropriate outgoing link and on to the next hop.

In this network scenario when a transmission request is made, control communication is initiated to allocate the required resources and establish a connection between two nodes (e.g. A and E as shown in Fig. 1). To tackle issues such as contention, bandwidth efficiency and capacity utilization while fulfilling the requirement for no buffering in the self-routing network, timing information is used to schedule the flows and reserve Lightwave Switched Paths (LSPs). After the transmission path is computed and all necessary resources are allocated, an optical header is embedded in the packet containing all nodes (tags) according to the computed path and the transmission commences. Upon arrival to the next node, the first tag is all-optically removed and the packet is forwarded to the appropriate outgoing link of the node by the control signals embedded within the specific tag "B", as in [7]. Equivalently, using the stacked tags as control signals within
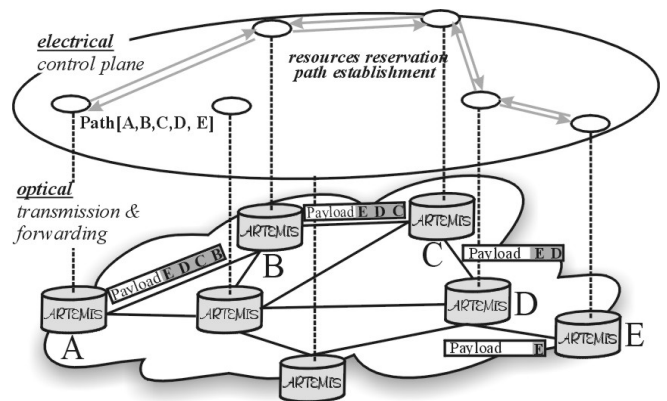

Fig. 1. ARTEMIS network architecture and all-optical burst forwarding.

each node, the packet is self-routed through until the destination node is reached and the packet is directed onto the "drop" port of "E".

B. Control Plane Design

Although self-routing is attractive due to the simplification of the routing control, the implementation of a buffer-less, all-optical network requires a suitable control plane design for the employment of contention control for traffic engineering. Standard methods to resolve this issue have been deflection routing and wavelength conversion, though both can result in complex routing either by increasing the network load or raising the hardware cost. Optical protocols [8] have been also proposed as a mean to provide contention protection, set the routing tables and configure the switches within the node. In the ARTEMIS concept, signaling mechanisms need to be employed to resolve common output port contention by communicating transmission periods, while the self-routing switching paradigm ensures correct intra-node switching. The ARTEMIS switch architecture is independent of the signaling protocol (protocol transparency) if prevention of contentions is ensured, however the use of timing information can be employed in order to reduce blocking and achieve high throughput. To exploit the advantages of using timely network state information, a switching node must be capable of recording the periods when its outgoing links are reserved as a function of time, usually referred to as the "utilization profile" of the node. In the proposed all-optical, self-routing network, where no buffering and wavelength conversion is utilized, a burst requests the full bandwidth of the core network C_{core}. We can represent the utilization profile of a link with a two-stated function of time with one state representing reserved periods of time (OFF) and the other state the free (ON).

C. Signaling Protocol Performance Evaluation

In this section we show that wait-for reservation and "tell-and-go" (TAG) type of flow and connection control protocols can be combined with the proposed switch architecture to meet the objectives of the ARTEMIS network concept. Two alternative solutions for resolving contention were theoretically investigated using the Network Simulator/NS2:
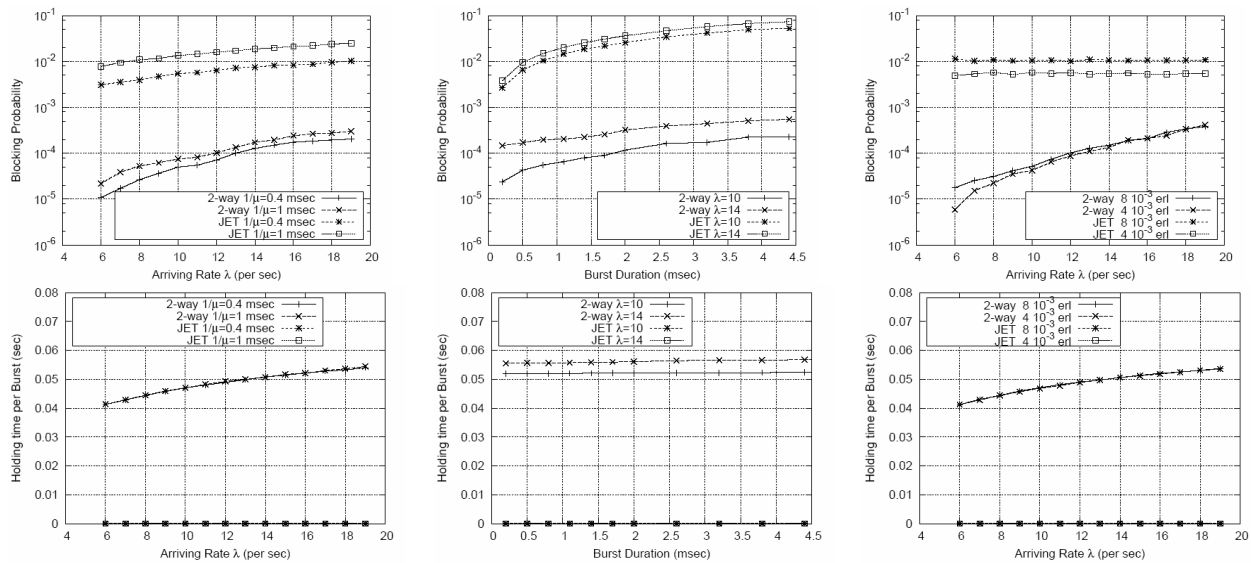
Fig. 2 (a) Blocking probability, (d) average holding time at network ingress nodes as function of Poisson arrival rate λ, for constant average burst duration values (1/μ). (b) blocking probability, (e) average holding time as function of average burst duration for constant λ values. (d) blocking probability, (f) average holding time as function of arrival rate λ for constant network offered load.

• One-way timed reservations and transmission of data after an offset time (JET signaling of the TAG category).

• Two-way timed reservations. The reservation of capacity is requested Trtt (round trip time) time after the arrival of the control packet, and when this cannot be provided a rejection packet is sent backwards to notify intermediate nodes and the source. The source node repeats the call setup, given a maximum holding time of data burst at the network edge.

We have employed a simple model for constructing the bursts, since burst aggregation is beyond the scope of this work. For the simulations, a dynamic traffic model was assumed in the form of burst transmission requests, which arrive at network edge nodes following a Poisson distribution with mean λ. Each request requires a one way connection to any other node with equal probability, resulting in uniformly distributed traffic load in the network. Burst transmission duration was assumed to follow a negative exponential distribution with mean value 1/μ. The simulation was conducted assuming the NSFNET backbone network topology. All links are assumed to be bi-directional, propagation delay is proportional to fiber length, processing delay is set to 0.02 msec and Ccore is equal to 40 Gb/s. Typical mean burst transmission durations that were considered (0.2-4 msec - correspond to burst sizes of 1-20 MBytes) are one order of magnitude less than the mean round trip time (Tmean-rtt=26 msec). Each edge router employs a virtual output queue to sort incoming packets on destination bases and the buffer size is set to 256 Mbytes. Dijkstra shortest path algorithm is used. In the 2-way reservation scheme a burst was dropped after remaining in edge node more than D=0.2 sec or if edge node buffer was overflowed. We used burst blocking probability and average holding time at the network edge as the main performance metrics. As holding time of a burst we define the time that the first bit of the burst is transmitted after burst assembly process.

Figures 2 (a), (d) show the blocking probability of the two

protocols as a function of the Poisson arrival rate (λ) for constant burst transmission durations (1/μ) and the corresponding holding times at the network edge points. Similar results were obtained for variations of 1/μ values for constant λ [Fig. 2(b) and (e)]. Finally, Fig. 2(d) and (f) show simulations carried out by maintaining the total network offered load constant (i.e 1/μ was adjusted to the given λ values to yield a constant product). These graphs show that the two-way protocol outperforms the TAG scheme concerning blocking probability, however at the expense of introducing delay at the network edges. The blocking performance of both protocols deteriorates as the offered load increases [increase of λ - Fig. 2(a), (d), or increase of mean 1/μ Fig. 2(b), (e)]. Figure 2(d) and (f) show that TAG performance depends only on the offered load, whereas the 2-way reservation protocol performance improves significantly when the offered load is provided in the form of fewer requests for larger bursts.

The results for both signaling schemes show that they can accommodate the all-optical routing in the ARTEMIS network by preventing contentions. The performance in terms of holding time and dropping probability validates the "protocol transparency" whereas combination can be applied to support variations in service traffic requirements.

III. ARTEMIS PHYSICAL LAYER NODE DESIGN AND ALL-OPTICAL SUBSYSTEM MODELING

The physical layer implementation of the ARTEMIS node is shown in Fig. 3 and consists of the self-synchronization stage, the all-optical header processing and the switching matrix. The synchronization stage provides the necessary clock signals that are self-extracted from the incoming data packets. The header processing/forwarding plane is responsible for all-optically processing the extracted tags and generating suitable control signals to drive the all-optical switching elements within the switching matrix. Here we describe the header format and all sub-systems required in order to realize such a photonic router.
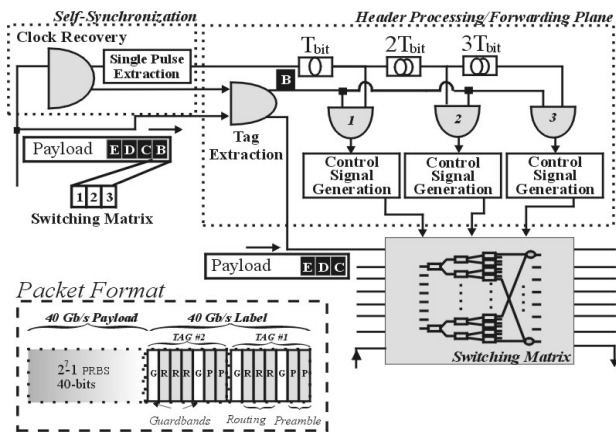
Fig. 3. ARTEMIS node physical layer implementation. Inset shows the packet format used for the simulation of ARTEMIS node operation consisting of two optical tags each containing three routing bits for controlling 8x8 switching matrices.

In each subsection the required functionality is identified and through physical layer modeling, an all-optical sub-system is proposed and modeled using the commercial simulation tool VPI TransmissionMaker. All proposed subsystems have been reported previously in experimental work performing either individually or as parts of more complex all-optical circuits.

A. ARTEMIS Packet Format

Figure 3 shows the packet format required for correct operation consisting of an optical label and payload both serially encoded at 40 Gb/s. The optical label comprises a number of stacked optical tags each representing an ARTEMIS node. The number of stacked tags depends on the number of hops within the network and they are embedded at the ingress node. Each tag contains a control signal that is a serially encoded binary word, used to set the switches within the node switching matrix. For the demonstration of ARTEMIS principle of operation, the packet format used in all simulation studies is shown in Fig. 3. The 40 Gb/s optical packet consists of a 40-bit long payload encoded with part of a 2^7-1 PRBS sequence. The label includes two stacked tags each containing binary routing bits and guardbands required by the synchronization and header processing stages of the node. Each tag has three embedded routing bits for controlling the switching matrix that consists of 1x2 optically-controlled gates. Two preamble bits are included at the start of each tag to assist the clock recovery process in each hop. Further, single-bit guardbands are inserted between each tag and payload as required by the tag extraction sub-system [2]. To investigate the cascadeability of the approach, the switching matrix was assumed to be a strictly non-blocking 8x8 switch, where each packet propagates through three cascaded 1x2 optical switching elements.

B. All-Optical Synchronization Stage

Figure 4 shows the schematic diagram of the proposed self-synchronization stage illustrating the two functionalities required, i.e. clock extraction at the line rate and single pulse extraction at the packet rate. The 40 Gb/s all-optical clock
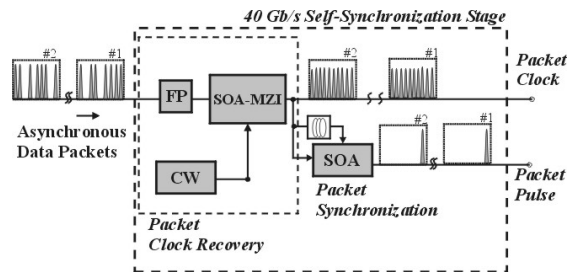

Fig. 4. Self-synchronization stage consisting of a 40 Gb/s packet clock recovery and a packet synchronization sub-system.
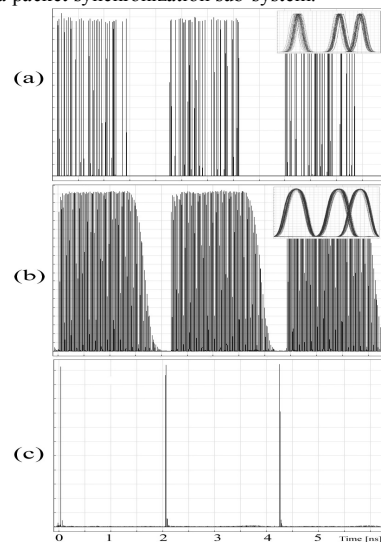

Fig. 5 (a) Incoming 40 Gb/s asynchronous data packets, (b) corresponding recovered clock packets and (c) extracted pulse per incoming packet at 500 ps/div timebase. Insets show asynchronous eye diagrams obtained.

recovery proposed [9] and simulated for the ARTEMIS node consists of a passive comb-generating filter for retiming and a saturated non-linear gate for reshaping. Combination of the two elements results in the self-extraction of clock packets suitable for controlling additional optical gates within the node. The reason for choosing this clock recovery scheme is the ability to perform per-packet clock extraction without requiring any synchronization to local optical or electrical oscillators leading to packet-format transparency. The comb-generating filter used was a Fabry-Perot filter with Finesse 20 and Free Spectral Range equal to the line rate. Exploiting the short memory effect of the filter, incoming data packets are transformed to clock-resembling packets. This signal, however, suffers from intense amplitude modulation that is removed by utilizing a saturated optical gate as a pulse-to-pulse equalizer [2]. The optical gate was simulated as a Semiconductor Optical Amplifier based Mach-Zehnder Interferometer (SOA-MZI) capable of operating at 40 Gb/s. The second synchronization subsystem is responsible for producing a single optical pulse per incoming data packet, without the intervention of any electronic circuitry. As shown in Fig. 4, this sub-system consists of a single SOA and exploits Cross Gain Modulation (XGM) effect to achieve the required
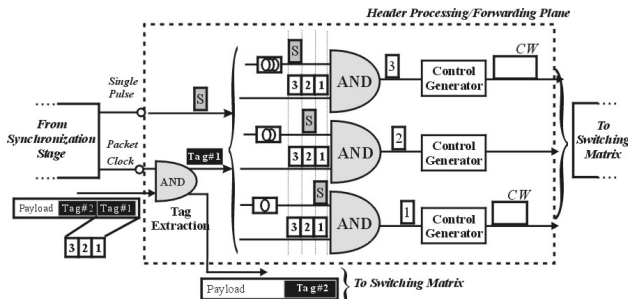
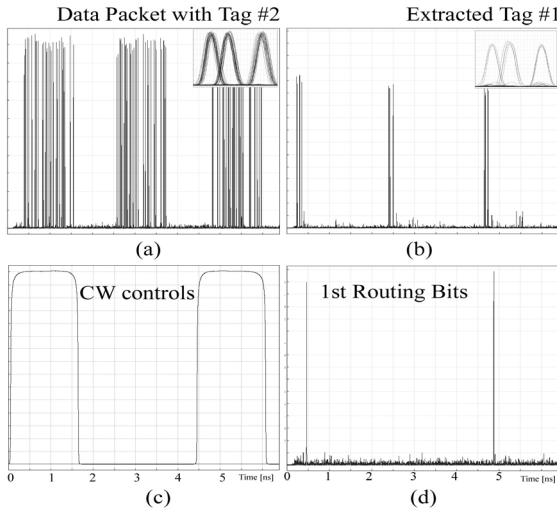Fig. 6. Schematic diagram of the header processing/forwarding plane.

Fig. 7. Simulation results of 40 Gb/s (a) extracted payload and remaining tag, (b) extracted tag #1, (c) generated CW control according to (d) extracted routing bit of each packet.

functionality. The recovered packet clock is inserted both as the probe and pump signal with a single bit offset in a counter-propagating fashion. Due to this temporal synchronization of the interacting signals, only the first pulse experiences amplification, whereas subsequent probe pulses are suppressed through the strong counter-propagating pump incident on the SOA. Figure 5 shows simulation results of the 40 Gb/s self-synchronization stage. Specifically, Fig. 5(a) illustrates three asynchronous packets with packet format according to section III.A, suffering from 0.8 dB and 500 fs amplitude and timing jitter respectively. When the incoming data enter the self-synchronization stage of the node, clock extraction on a per-packet basis is achieved. Hence, a packet clock with instant locking [9] and short decay time is extracted from each incoming packet as shown in Fig. 5(b). Finally, the extracted clock packets are inserted into the packet synchronizer and a single pulse per incoming packet is generated at the output [Fig 5(c)]. The extracted clock packets exhibited 0.25 dB and 277 fs amplitude and timing jitter. The extracted optical pulse was measured to have extinction ratio of more than 14 dB.

C. All-Optical Header Processing/Forwarding Plane

This part of the node includes three all-optical functionalities: tag extraction, routing bit extraction and control signal generation. The principle of operation of the header processing

plane is presented in Fig. 6. The incoming optical packet and the recovered packet clock stream enter the tag extraction gate that consists of a SOA-MZI configured as a Boolean AND [2]. The temporal synchronization of the two signals is such that the first optical tag (Tag #1) lies outside the switching window defined by the recovered clock. Hence, the whole payload, including Tag #2, is switched, whereas only Tag #1 remains unswitched and enters the header processing/forwarding plane. Having separated the optical tag from the remaining payload, the optical tag is then fed into an array of SOA-MZIs, each responsible for extracting a single routing bit, using the extracted single pulse. The single pulse is synchronized with the optical tag at the input of each SOA-MZI gate. By imposing a single bit of optical delay to the single pulse that is fed as control signal, a single routing bit is switched at the output of each optical gate. Finally, each routing bit enters the control signal generation block and depending on its binary value, a control signal is generated and forwarded to the switching matrix. The optical functionality required in the control signal generator is the transformation of bit-level signal into a packet-level signal by exploiting an optical element exhibiting memory. Hence, a single optical bit at the input of the control signal generator must be capable of producing a CW or pulsed block with duration equal to the total packet length, as shown in Fig. 6. There are three ways of implementing such a control signal generator using an optical flip-flop [3], an optical circuit with finite memory [10] or an electronic pulse generator followed by optoelectronic conversion [6]. To reduce the complexity of the simulation model, the control signal generator was implemented as in [6]. The complete header processing plane was simulated and Fig. 7 shows results obtained at 40 Gb/s. Figures 7(a) and (b) show the two outputs of the tag extraction optical gate. Figure 7(a) shows the packet payload with remaining tags appearing at the un-switched port of the gate. Figure 7(b) shows the extracted Tag #1 appearing at the switched port of the gate due to the interaction with the extracted packet clock. According to the principle of operation of the node forwarding functionality, each routing bit embedded within the tag is removed by the routing bit extraction gates. Figure 7(d) shows the output of the first optical gate that performs an AND operation between the single pulse and the first routing bit in each packet tag. Depending on the value of each routing bit, a CW control signal is generated as shown in Fig. 7(c). These generated CW signals are used to control the all-optical 1x2 optical elements of the switching matrix described in the next section.

D. All-Optical Switching Matrix

The fundamental building block of the switching matrix is a 1x2 optically addressable switch implemented with SOA-MZIs. Figure 8 shows the 8x8 strictly non-blocking architecture. The propagation path of each data packet within the array of interconnected gates depends on the CW control signals generated at the header processing plane. At each stage, the CW control block changes the state of the 1x2 switch into cross-state and the packet is switched accordingly. All incoming data packets are self-routed through the matrix in completely independent optical paths to avoid internal
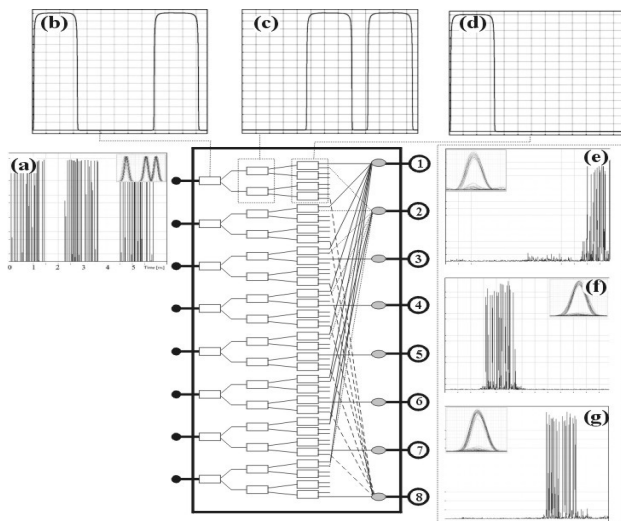
Fig. 8. ARTEMIS 8x8 switching matrix showing (a) incoming 40 Gb/s asynchronous packets, (b), (c), (d) corresponding control signals generated and (e), (f), (g) self-routed packets at the switch output.
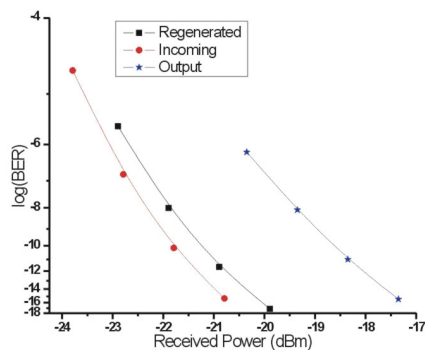

Fig. 9. Bit Error Rate measurements for back-to-back, output of the 8x8 node and after 2-stage. 2R regeneration.

contention. At the output stage, the optical paths are coupled using 8x1 fiber couplers forming the outgoing links of the switching matrix. The architecture is strictly non-blocking, ensuring that no internal blocking occurs for input packets that different output ports. On the other hand, the signaling algorithm also ensures that two incoming data packets do not request the same outgoing link, allowing for each output stage of the matrix to be coupled without causing contention.

The theoretical studies for the switching matrix were focused on the noise performance due to cascaded SOA-MZI gates. To investigate the signal degradation of the optical packets, the simulation was used to model the propagation of the signal through the optically controlled 1x2 switches. Figure 8(a) shows the incoming 40 Gb/s stream consisting of three packets, each requesting a specific outgoing link. Figure 8(b)-(d) show pulse traces of the generated control signals for all packets at each stage in the switching matrix and Fig. 8(e)-(g) show the self-routed packets and corresponding eye diagrams. Figure 9 shows BER measurements carried out to investigate the penalty induced due to signal propagation through cascaded optical switches. The results show a 3.8 dB penalty for the complete self-router which is compensated to 0.5 dB through standard 2R regeneration at the output of the node.

IV. CONCLUSIONS

We have demonstrated a self-routing network and node architecture and validated the concept through network studies and node physical layer simulations. We showed successful self-routing of 40 Gb/s asynchronous optical packets by modeling a complete 8x8 ARTEMIS node. We also applied signaling mechanisms to provide contention prevention is achieved in the ARTEMIS network.

V. ACKNOWLEDGEMENT

REFERENCES

[1] F. Ramos et al., "IST-LASAGNE: Towards All-Optical Label Swapping Employing Optical Logic Gates and Optical Flip-flops," submitted to *IEEE/OSA J. Lightwave Technol.*, Special Issue on Optical Networks.

[2] E. Kehayas, et al., "Packet-Format and Network-Traffic Transparent Optical Signal Processing", *IEEE/OSA J. Lightwave Technol.*, Special Issue on Metro & Access Networks, Vol. 22, pp. 2548-2556, Nov. 2004

[3] M. T. Hill et al. "All-optical flip-flop based on coupled laser diodes", *IEEE J. Quantum Electron.*, vol. 37, pp. 405-413, March 2001.

[4] S.-W. Seo et al., "Bit-level packet-switching all-optical multihop shuffle networks with deflection routing", *Applied Optics*, Vol. 36, pp. 3142-3146, May 1997.

[5] J.-G. Zhang. "Optically self-clocked and self-routing photonic bit switch using pulse-interval encoding", *Pure Appl. Opt.*, Vol. 2, pp. 411-418, Sept. 1993.

[6] T. Nakahara et al, "Time-Domain 16-bit Label Swapping and Self-Routing of 40-Gb/s Burst Optical Packets", *IEEE Photon. Terchnol. Lett.*, Vo. 16, pp. 2153-2155, Sept. 2004.

[7] R. Van Caenegem et al., "All-Optical Label Swapping Versus Label Stripping: A Node Dimensioning Point of View," *European Conference on Optical Communication*, 2004, Th3.6.3, Stockholm, Sweden.

[8] J. Teng and G. N. Rouskas, "A Comparison of the JIT, JET, and Horizon Wavelength reservation Schemes on A Single OBS Node,", *1st International Workshop on Optical Burst Switching*, Oct. 2003, Dallas.

[9] E. Kehayas, et al., "40 Gb/s all-optical packet clock recovery with ultrafast lock-in time and low inter-packet guardbands," *OSA Opt. Express*, Vol. 13, pp. 475-480, Jan. 2005.

[10] K. Yiannopoulos, et al., "Generation of 40-GHz control signals from flag pulses for switching all-optical gates for use with optical packets", *OSA Opt. Lett.*, Vol. 29, pp. 241-243, Feb. 2004.