COURSE OUTLINE

(1) GENERAL

<table>
<thead>
<tr>
<th>SCHOOL</th>
<th>Engineering</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACADEMIC UNIT</td>
<td>Department of Computer Engineering &amp; Informatics</td>
</tr>
<tr>
<td>LEVEL OF STUDIES</td>
<td>Undergraduate</td>
</tr>
<tr>
<td>COURSE CODE</td>
<td>CEID_NE4617</td>
</tr>
<tr>
<td>SEMESTER</td>
<td>winter semester</td>
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</tbody>
</table>

INDEPENDENT TEACHING ACTIVITIES

if credits are awarded for separate components of the course, e.g. lectures, laboratory exercises, etc. If the credits are awarded for the whole of the course, give the weekly teaching hours and the total credits.

<table>
<thead>
<tr>
<th>WEEKLY TEACHING HOURS</th>
<th>CREDITS</th>
</tr>
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<tbody>
<tr>
<td>Lectures and tutorials, Laboratory exercises</td>
<td>3, 2</td>
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</tbody>
</table>

Add rows if necessary. The organisation of teaching and the teaching methods used are described in detail at (d).

<table>
<thead>
<tr>
<th>COURSE TYPE</th>
<th>Specialized general knowledge, Skills development</th>
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PREREQUISITE COURSES:

Proposed background knowledge:
- Introduction to Computers and Programming (NY131)
- Digital Design I (NY163)
- Digital Design II (NY164)
- Basic Topics in Computer Architecture (NY261)
- Modern Topics in Computer Architecture (NY262)

LANGUAGE OF INSTRUCTION and EXAMINATIONS:

Greek

IS THE COURSE OFFERED TO ERASMUS STUDENTS

No

COURSE WEBSITE (URL)

https://eclass.upatras.gr/courses/CEID1027/

2. LEARNING OUTCOMES

Learning outcomes
The course learning outcomes, specific knowledge, skills and competences of an appropriate level, which the students will acquire with the successful completion of the course are described.

Consult Appendix A

- Description of the level of learning outcomes for each qualifications cycle, according to the Qualifications Framework of the European Higher Education Area
- Descriptors for Levels 6, 7 & 8 of the European Qualifications Framework for Lifelong Learning and Appendix B
- Guidelines for writing Learning Outcomes

Upon the successful finalization of this course, the students will be able to:

- Analyze and assess the various datapath configurations of modern processors
- Understand different processor architectures and system-level design processes
- Understand the Moore’s law and the Dennard’s scaling law
- Understand the basic components of power consumption in CMOS technologies
- Understand and assess the mechanisms of dynamic and speculative instruction execution
- Tomasulo algorithm
- Static and dynamic branch prediction techniques
- Two-level branch predictors (m, n)
- Dynamic register renaming
- Predication technique
- Case studies: Core Duo and Itanium (Intel)
- Understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
- Hardware level cache based optimizations
- Victim caches, pseudo-associative caches, elbow caches
- Hardware-software optimizations (replacement strategies, prefetching)
- Analysis of the usage of trace cache in hyperthreading architectures
- Compiler level cache optimizations (loop transformations)
- Instruction and data prefetching techniques at the hardware, compiler, and software levels
- Understand the organisation and operation of current generation parallel computer systems, including
The transition to multicore architectures (ILP wall + power wall + memory wall = multicores)
- SISD, SIMD, MISD, MIMD architectures
- Shared memory architectures
- The cache coherency problem
- Directory based and snooping/broadcast protocols
- False sharing elimination techniques
- Categories and types of multithreaded architectures
- The CUDA GPGPU programming model
- Memory ordering and memory consistency models (sequential, relaxed, weak consistency models)
- Memory synchronization through atomic load/stores instructions
- Other types of parallelism like helper threads, thread level speculation via speculative precomputation and/or run-ahead execution) and transactional memories.

General Competences
Taking into consideration the general competences that the degree-holder must acquire (as these appear in the Diploma Supplement and appear below), at which of the following does the course aim?

- Search for, analysis and synthesis of data and information, with the use of the necessary technology
- Adapting to new situations
- Decision-making
- Working independently
- Team work
- Working in an international environment
- Working in an interdisciplinary environment
- Production of new research ideas
- Production of free, creative and inductive thinking
- Adapting to new situations
- Decision-making
- Working independently
- Team work
- Working in an international environment
- Production of new research ideas
- Production of free, creative and inductive thinking

3. Syllabus

The key topics addressed are:
- Basic principles of 5-stage pipeline
  - Single-cycle architectures
  - Multi-cycle pipeline architectures
- Analysis of Moore’s law and Dennard’s scaling law
  - Principal of power consumption in CMOS technology
  - The transition from uncore to multicore architectures
- Dynamic and speculative instruction execution
  - Tomasulo algorithm
  - Static and dynamic branch prediction techniques
  - Two-level branch predictors (m, n)
  - Dynamic register renaming
  - Predication technique
  - Case studies: Core Duo and Itanium (Intel)
- Hardware level cache based optimizations
  - Victim caches, pseudo-associative caches, elbow caches
  - Hardware-software optimizations (replacement strategies, prefetching)
  - Analysis of the usage of trace cache in hyperthreading architectures
- Compiler level cache optimizations (loop transformations)
- Instruction and data prefetching techniques at the hardware, compiler, and software levels
- Multicore architectures
  - The transition to multicores (ILP wall + power wall + memory wall = multicores)
  - SISD, SIMD, MISD, MIMD architectures
  - Shared memory architectures
  - The cache coherency problem
  - Directory based and snooping/broadcast protocols
  - False sharing elimination techniques
  - Categories and types of multithreaded architectures
  - The CUDA GPGPU programming model
• Memory ordering and memory consistency models (sequential, relaxed, weak consistency models)
• Memory synchronization through atomic load/stores instructions
• Other types of parallelism like helper threads, thread level speculation via speculative precomputation and/or run-ahead execution) and transactional memories.

4. TEACHING and LEARNING METHODS - EVALUATION

<table>
<thead>
<tr>
<th>DELIVERY</th>
<th>Face-to-face, Distance learning, etc.</th>
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</table>
| USE OF INFORMATION AND COMMUNICATIONS TECHNOLOGY | ICT technologies are widely used throughout the course. In particular:
- There are separate webpages for the lectures and the laboratory exercises that host all the required material.
- The communication with the students is mainly performed via emails and by using the announcement facilities of eclass. |

<table>
<thead>
<tr>
<th>TEACHING METHODS</th>
<th>Use of ICT in teaching, laboratory education, communication with students</th>
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<tbody>
<tr>
<td>The manner and methods of teaching are described in detail. Lectures, seminars, laboratory practice, fieldwork, study and analysis of bibliography, tutorials, placements, clinical practice, art workshop, interactive teaching, educational visits, project, essay writing, artistic creativity, etc. The student’s study hours for each learning activity are given as well as the hours of non-directed study according to the principles of the ECTS.</td>
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<table>
<thead>
<tr>
<th>Activity</th>
<th>Semester workload</th>
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<tbody>
<tr>
<td>Διαλέξεις</td>
<td>26 hours</td>
</tr>
<tr>
<td>Φροντιστήριο</td>
<td>13 hours</td>
</tr>
<tr>
<td>Εκπόνηση εργαστηριακών ασκήσεων</td>
<td>26 hours</td>
</tr>
<tr>
<td>Προετοιμασία εργαστηριακών ασκήσεων</td>
<td>13 hours</td>
</tr>
<tr>
<td>Συγγραφή αναφορών εργαστηριακών ασκήσεων</td>
<td>10 hours</td>
</tr>
<tr>
<td>Μελέτη</td>
<td>50 hours</td>
</tr>
<tr>
<td>Εξετάσεις θεωρίας</td>
<td>3 hours</td>
</tr>
<tr>
<td>Εξετάσεις εργαστηριακής ενότητας</td>
<td>1 hours</td>
</tr>
</tbody>
</table>

| Course total | 142 hours |

5. ATTACHED BIBLIOGRAPHY

- Προτεινόμενη Βιβλιογραφία:
  - Computer Architecture: A Quantitative Approach, Hennessy John L., Patterson David A.
  - Structured Computer Organization, ANDREW S. TANENBAUM

- Συναφή επιστημονικά περιοδικά:
  - IEEE Micro
  - IEEE Transactions on Computers
  - IEEE Transactions on VLSI Systems
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems