COURSE OUTLINE

(1) GENERAL

<table>
<thead>
<tr>
<th>SCHOOL</th>
<th>Engineering</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACADEMIC UNIT</td>
<td>Department of Computer Engineering &amp; Informatics</td>
</tr>
<tr>
<td>LEVEL OF STUDIES</td>
<td>Undergraduate</td>
</tr>
<tr>
<td>COURSE CODE</td>
<td>CEID_5668</td>
</tr>
<tr>
<td>SEMESTER</td>
<td>spring semester</td>
</tr>
<tr>
<td>COURSE TITLE</td>
<td>Special Topics in Digital Systems Design</td>
</tr>
</tbody>
</table>

INDEPENDENT TEACHING ACTIVITIES

<table>
<thead>
<tr>
<th>WEEKLY TEACHING HOURS</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lectures and tutorials, Laboratory exercises</td>
<td>3(L), 2(LE)</td>
</tr>
</tbody>
</table>

Add rows if necessary. The organisation of teaching and the teaching methods used are described in detail at (d).

<table>
<thead>
<tr>
<th>COURSE TYPE</th>
<th>Specialized general knowledge</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Skills development</td>
</tr>
</tbody>
</table>

PREREQUISITE COURSES:

1. Introduction to Computers and Programming (NY131)
2. Digital Design I (NY163)
3. Digital Design II (NY164)
4. Basic Topics in Computer Architecture (NY261)
5. Introduction to VLSI (NE4648)

LANGUAGE OF INSTRUCTION and EXAMINATIONS: Greek

IS THE COURSE OFFERED TO ERASMUS STUDENTS: No

COURSE WEBSITE (URL): https://eclass.upatras.gr/courses/CEID1013/

(2) LEARNING OUTCOMES

Learning outcomes

The course learning outcomes, specific knowledge, skills and competences of an appropriate level, which the students will acquire with the successful completion of the course are described.

Consult Appendix A

- Description of the level of learning outcomes for each qualifications cycle, according to the Qualifications Framework of the European Higher Education Area
- Descriptors for Levels 6, 7 & 8 of the European Qualifications Framework for Lifelong Learning and Appendix B
- Guidelines for writing Learning Outcomes

A. Lectures and Tutorials

Upon successful completion of the course, a student will:

- know the need for testing
- know the difference between verification testing and manufacturing testing
- be familiar with parametric, functional and structural logic testing
- know the problems and the economics of testing
- know the current fault models
- be familiar with several types of fault simulation and test pattern generation algorithms
- know several Design For Testability (DFT) methods (General guidelines, test point insertion, Pseudoexhaustive testing, Scan Path Design Techniques, Built-In Self-Test (BIST) techniques, Test Data Compression techniques)
- know the fault models which are suitable for testing semiconductor memories
- know the standards IEEE Std. 1149.1) and IEEE STD 1500 for testing boards and embedded cores in SOCs

B. Laboratory Exercises

Upon successful completion of the course, a student will be able to:
• using open source code tools as well as commercial tools to derive the test set of a circuit and to do
  fault simulation
• insert test points
• design BIST techniques
• insert scan paths

General Competences
Taking into consideration the general competences that the degree-holder must acquire (as these appear in the
Diploma Supplement and appear below), at which of the following does the course aim?

Search for, analysis and synthesis of data and technology
Adapting to new situations
Decision-making
Working independently
Team work
Working in an international environment
Working in an interdisciplinary environment
Production of new research ideas

Adapting to new situations
Decision-making
Working independently
Team work
Working in an international environment
Production of new research ideas

(3) Syllabus

• Introduction:
  ✓ The need for testing
  ✓ Verification testing vs. manufacturing testing
  ✓ Parametric testing
  ✓ Logic testing
    ✗ Functional testing
    ✗ Structural testing
  ✓ periodic testing,
  ✓ Test issues
  ✓ Problems of testing
  ✓ Test economics

• Part I. TESTING
  ✓ Failures, Defects and Fault Models:
    ✗ Terminology
    ✗ Failure Classification
    ✗ Failure Rate Vs Product Lifetime
    ✗ Fault models: Stuck-at Faults, Bridging Faults, Stuck-Open Faults, Delay Faults
  ✓ Fault Simulation:
    ✗ Logic simulation versus Fault simulation
    ✗ Fault Simulation, Fault Coverage
    ✗ Fault Dictionary
    ✗ Compiled versus event driven simulators
    ✗ Several implementations (Serial, Parallel, Deductive and Concurrent fault simulators)
  ✓ Testability Measures (SCOAP),
  ✓ Test Pattern Generation:
    ✗ Exhaustive
    ✗ Pseudoexhaustive
    ✗ Pseudorandom (PR)
    ✗ Deterministic (D-Algorithm, PODEM, FAN Fujiwara, Critical paths) tests.

• Part II. DESIGN FOR TESTABILITY (DFT)
  ✓ General guidelines
  ✓ test point insertion
  ✓ Pseudoexhaustive testing,
  ✓ Scan Path Design Techniques:
    ✗ Types of storage devices
(4) TEACHING and LEARNING METHODS - EVALUATION

<table>
<thead>
<tr>
<th>DELIVERY</th>
<th>Face-to-face, Distance learning, etc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>USE OF INFORMATION AND COMMUNICATIONS TECHNOLOGY</td>
<td>Wide use of ICT. More specifically:</td>
</tr>
<tr>
<td>Use of ICT in teaching, laboratory education, communication with students</td>
<td>• The course is backed up by a web page for the lectures and the tutorials and a second e-class page providing all necessary documentation for the laboratory exercises.</td>
</tr>
<tr>
<td>• The preferred communication method with the students is email.</td>
<td></td>
</tr>
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<table>
<thead>
<tr>
<th>TEACHING METHODS</th>
<th>Activity</th>
<th>Semester workload</th>
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</thead>
<tbody>
<tr>
<td>The manner and methods of teaching are described in detail. Lectures, seminars, laboratory practice, fieldwork, study and analysis of bibliography, tutorials, placements, clinical practice, art workshop, interactive teaching, educational visits, project, essay writing, artistic creativity, etc. The student’s study hours for each learning activity are given as well as the hours of non-directed study according to the principles of the ECTS.</td>
<td>Lectures</td>
<td>26 hours</td>
</tr>
<tr>
<td></td>
<td>Tutorials</td>
<td>13 hours</td>
</tr>
<tr>
<td></td>
<td>Laboratory exercises</td>
<td>26 hours</td>
</tr>
<tr>
<td></td>
<td>Laboratory exercises preparation</td>
<td>13 hours</td>
</tr>
<tr>
<td></td>
<td>Report preparation</td>
<td>13 hours</td>
</tr>
<tr>
<td></td>
<td>Study</td>
<td>52 hours</td>
</tr>
<tr>
<td></td>
<td>Theory exams</td>
<td>3 hours</td>
</tr>
<tr>
<td></td>
<td>Laboratory exams</td>
<td>1 hour</td>
</tr>
<tr>
<td></td>
<td>Course total</td>
<td>147 hours</td>
</tr>
</tbody>
</table>

| STUDENT PERFORMANCE EVALUATION | |
| Description of the evaluation procedure | The evaluation is performed in Greek language and is based on two independent parts. |
| Language of evaluation, methods of evaluation, summative or conclusive, multiple choice questionnaires, short-answer questions, open-ended questions, problem solving, written work, essay/report, oral examination, public presentation, laboratory work, clinical examination of patient, art interpretation, other | The theory evaluation is performed through a final written test that includes multiple choice questions, short-answer questions and problem solving. After the test marks are announced, the students have the opportunity to see their mistakes. |
| Specifically-defined evaluation criteria are given, and if and where they are accessible to students. | The evaluation for the laboratory part is based on: |
| • the correctness of the designs made by the students |
| • the quality of documenting the designs |

(5) ATTACHED BIBLIOGRAPHY

- Προτεινόμενη Βιβλιογραφία:
- VLSI Testing and Design for Testability, Notes, Δ. Νικολός

- Συναφή επιστημονικά περιοδικά:
  - IEEE Design & Test of Computers
  - IEEE Transactions on Computers,
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
  - IEEE Transactions on VLSI Systems.