

Gallium Arsenide Technology

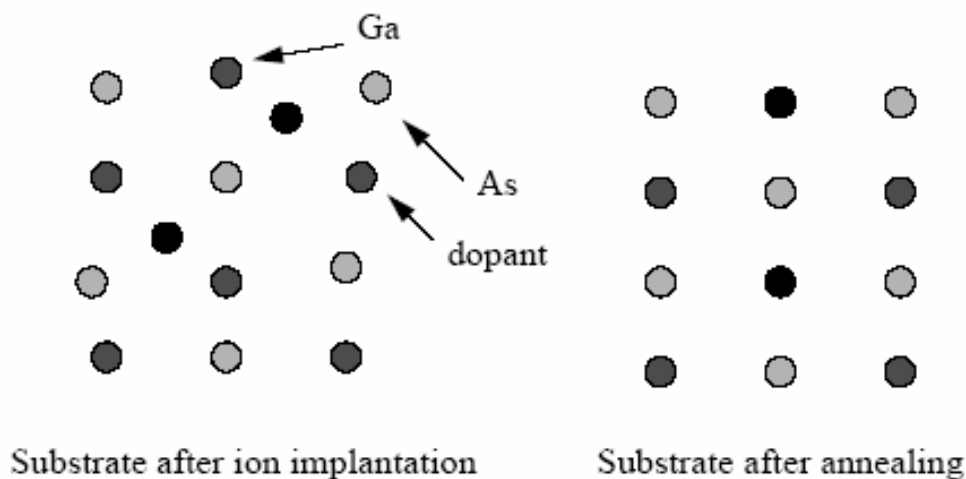
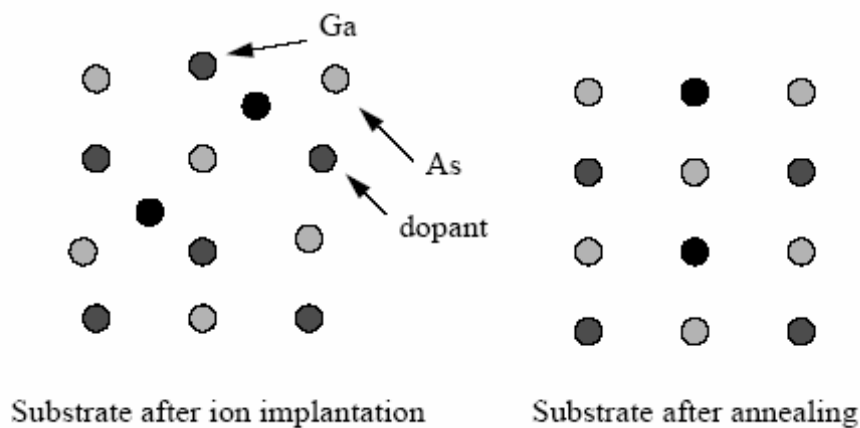
Outline

- GaAs Introduction
- Advantages compared to silicon
- MESFET technology
- E/D MESFET operation and models
- Logic Classes: DCFL, SDCFL
- examples of fabricated chips

Shortcomings in Silicon based technologies have moved researchers to explore other semi-conductors from which **faster** and **lower power** devices can be made.

Gallium Arsenide or 'GaAs' is a compound semi-conductor made from Gallium (group III) and Arsenic (group V) elements.

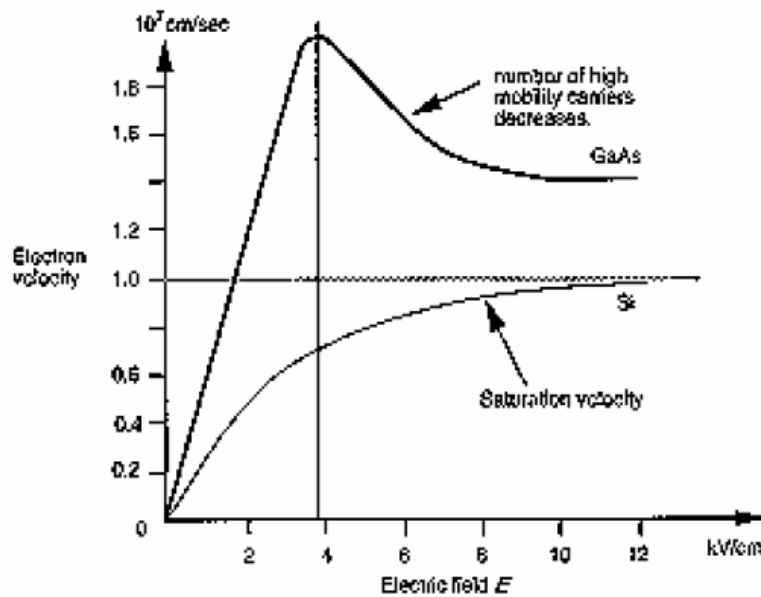
- Group IV elements (Si) are used as dopants to displace and replace a Gallium site to form an n-type region. Note a Ga atom can replace a As site to form p-type material but after annealing, the material is n-type since the As atoms are smaller than both Si and Ga atoms.



- Group II (Mg or Be) are used to form p-type regions but since they are heavy elements, they damage the GaAs lattice structure.
- GaAs was grown and chemically characterised in 1926 and is used more widely in the 1990's as processing techniques improve.
- Most GaAs circuits fabricated have been for MMICs or detectors (temperature).

Characteristics - compared to Si.

- The saturated electron drift velocity of GaAs is ~ 2 times Silicon at lower electric field strengths due to a small valence band gap.



- This means GaAs devices require less voltage to enter saturation.
 - The mobility of electrons in GaAs is 6-7 times that of Silicon resulting in very fast electron transit times.
-
- Intrinsic bulk resistivities are higher (GaAs= 10^8 , Si= $2.2 \times 10^5 \Omega \cdot \text{cm}$) which minimises parasitic capacitances and allows easy isolation of multiple devices in a single substrate.
 - Higher radiation resistance because there is no gate oxide to trap charges.
 - Wider operating temperature due to wider bandgap ($\pm 200^\circ\text{C}$)
 - Better photo-response than Si.
 - Substrate is more brittle than Si and therefore thicker.
 - mobility is dependent on direction in crystal planes, so layout devices with gates all in one direction to maximise mobility.
 - mobility of holes in GaAs is slightly worse than that of Silicon, so p-type devices in GaAs are large and slow. Therefore complementary GaAs structures have been unpopular.

GaAs Devices

The **first generation** of GaAs devices included:

- depletion mode MESFET (Metal Semiconductor FET)
- enhancement mode MESFET
- enhancement mode JFET
- complementary enhancement mode FET (CE-JFET)

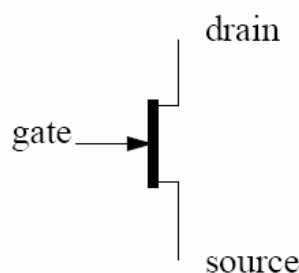
These devices have switching delays as low as 50ps for between 1 and 2.5mW power dissipation. MESFETs have been the mainstay of digital GaAs circuits.

The **second generation** devices include

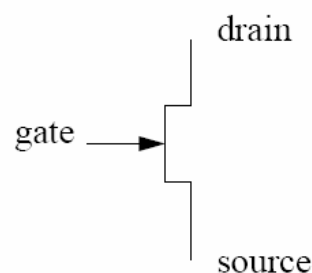
- high electron mobility transistor (HEMT)
- heterojunction bipolar transistor (HJBT)

Electron mobility in the second generation is up to 5 times higher than the first generation and are mostly used for analog circuits such as low noise RF amplifiers.

A recent innovation in device design has led to the introduction of complementary HEMT devices, i.e. p-devices with much better mobility than previous device generations which allows CMOS-like structures to be made.



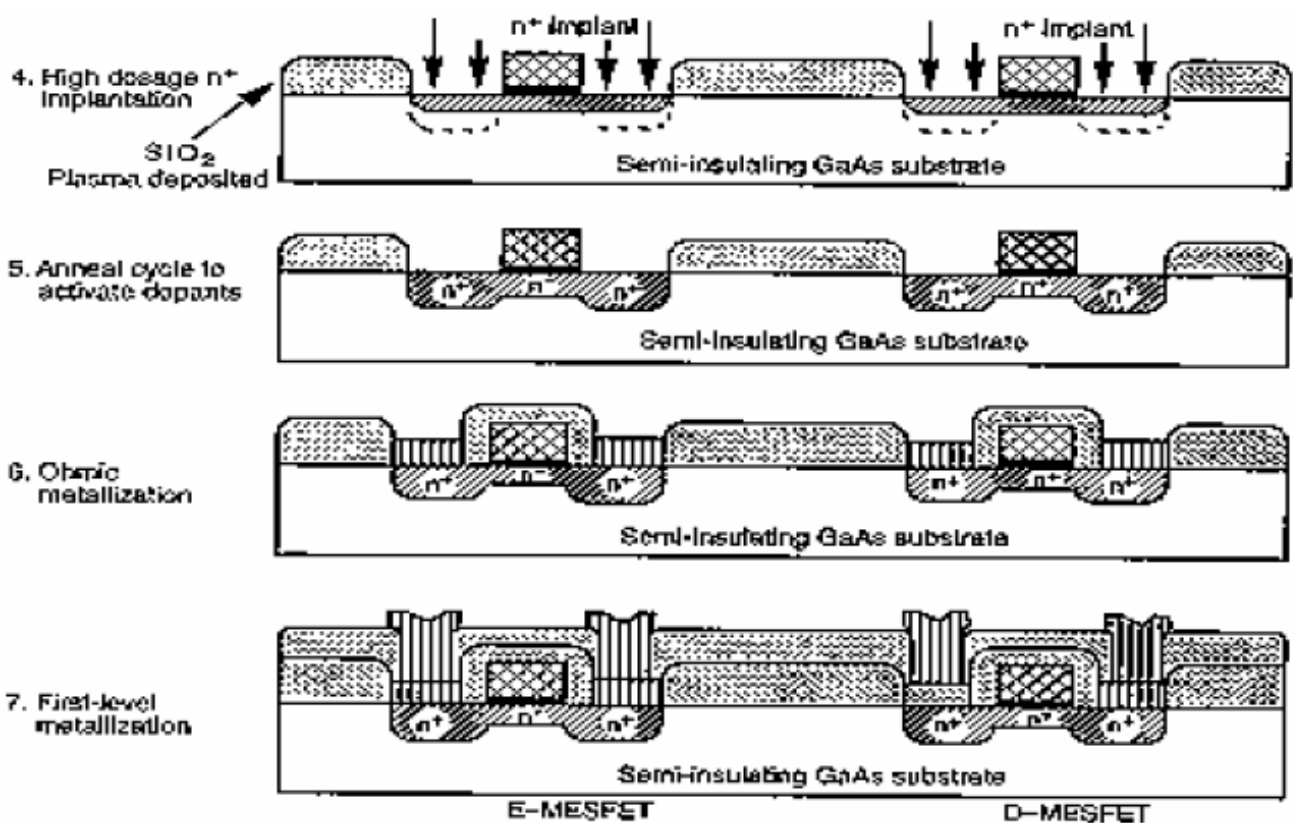
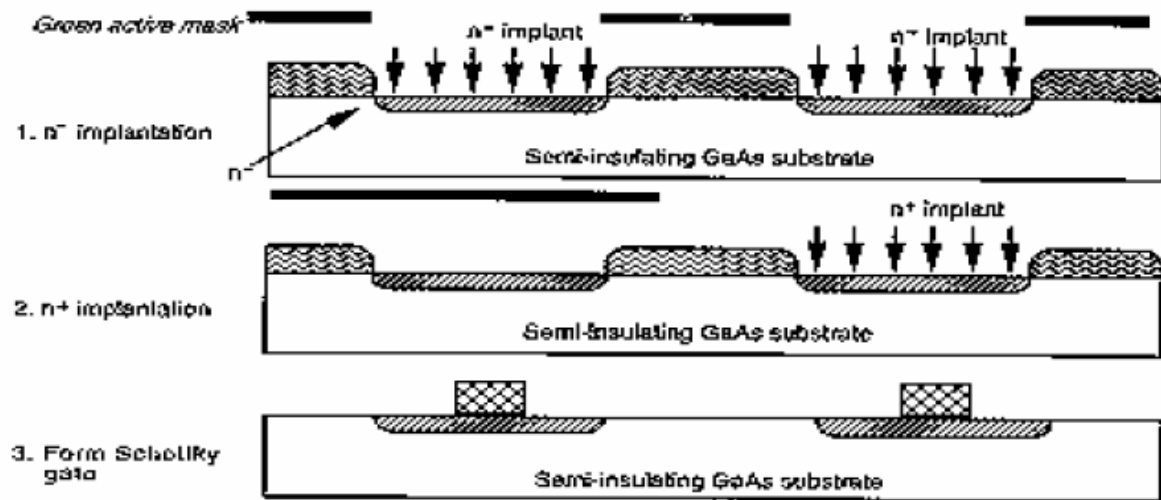
D-MESFET



E-MESFET

GaAs MESFET Technology

- The MESFET is a bulk-current conduction majority carrier device.
- It is fabricated from bulk GaAs by ion implantation and high-resolution photolithography.



positive V_t

negative V_t

MESFET Operation

- The channel in a MESFET is formed by doping the GaAs substrate (different doping concentrations and profiles for E and D devices).
- A depletion region extends only part way through the channel for a depletion device (highly doped thick channel) and all the way through for an enhancement device (lightly doped thin channel).
- MESFETs are similar in operation to MOSFETs except for a Schottky diode formed at the gate junction, the capacitance of which is used to control the effective charge in the channel.
- A Schottky diode has a built-in barrier height voltage ($\Phi_B \approx 0.7 - 0.8V$).
- The threshold voltage is given by: $V_t = \Phi_B - V_{PO}$ where V_{PO} is the pinch-off voltage.

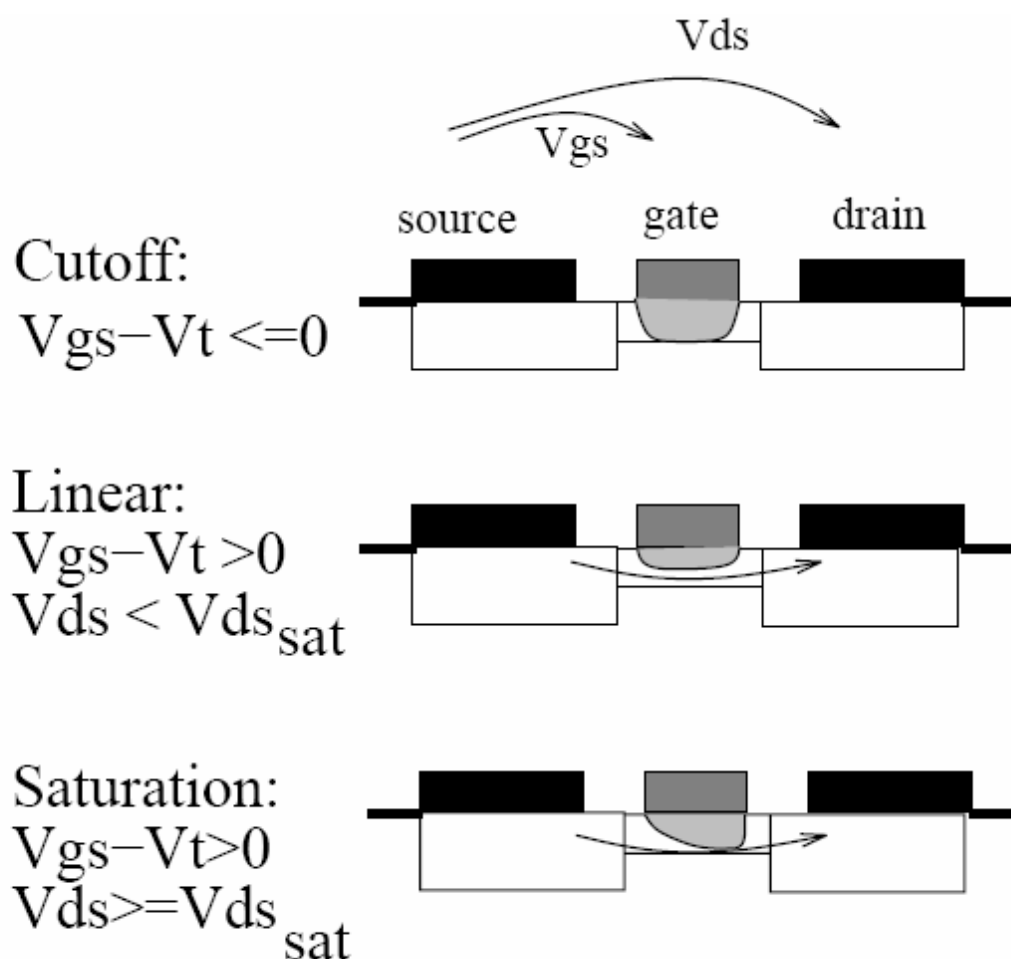
- The pinch-off voltage, V_{PO} is simply the total voltage, both built-in potential voltage and externally applied voltage necessary to completely deplete the channel of mobile charge carriers.

$$V_{PO} = \frac{qN_d a^2}{2\epsilon_r \epsilon_0}$$

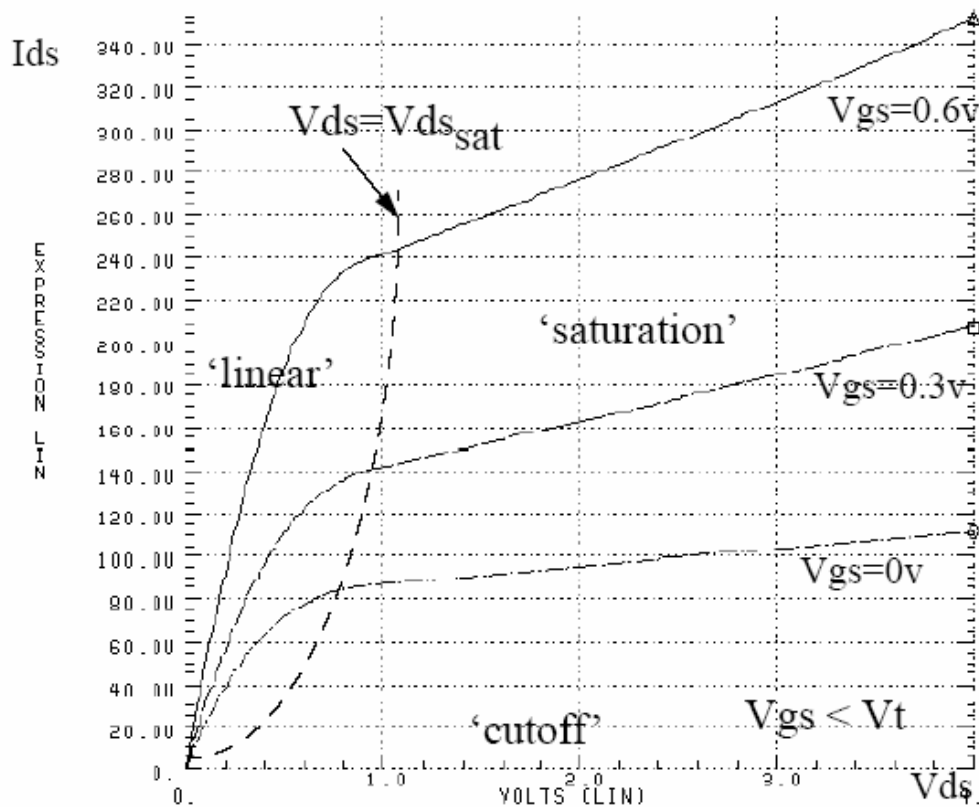
- where a is the channel thickness of the n-implant, N_d is the effective channel concentration density and $\epsilon_r = 13.1$ for GaAs.
- The maximum gate-to-source voltage (V_{gs}) is $\sim 0.8V$, above which it is clamped due to forward conduction of the Schottky diode.
- With voltage swings of around $0.5V$, the variation of threshold voltage across a chip should be controlled to less than 5% of the voltage swing (i.e. $25mV$ for an E-MESFET).

The drain current in a MESFET is controlled by V_{gs} and V_{ds} and the device has three regions of operation.

- **cutoff**, where the channel is completely cut off by the depletion region which extends into the channel. This occurs when the external bias voltage applied to the Schottky diode is less than the threshold voltage ($V_{gs} - V_t \leq 0$).
- **linear or ohmic**, where there is a voltage applied to V_{gs} above the threshold voltage ($V_{gs} - V_t > 0$), and V_{ds} is positive and less than the drain-source saturation voltage, $V_{ds_{sat}}$. The drain current is linear with V_{ds} in this region so the channel acts as a resistor.
- **saturation**, if $V_{gs} - V_t > 0$ and $V_{ds} > V_{ds_{sat}}$, the depletion region becomes wedge shaped and the channel becomes pinched off at the drain end limiting the flow of current.



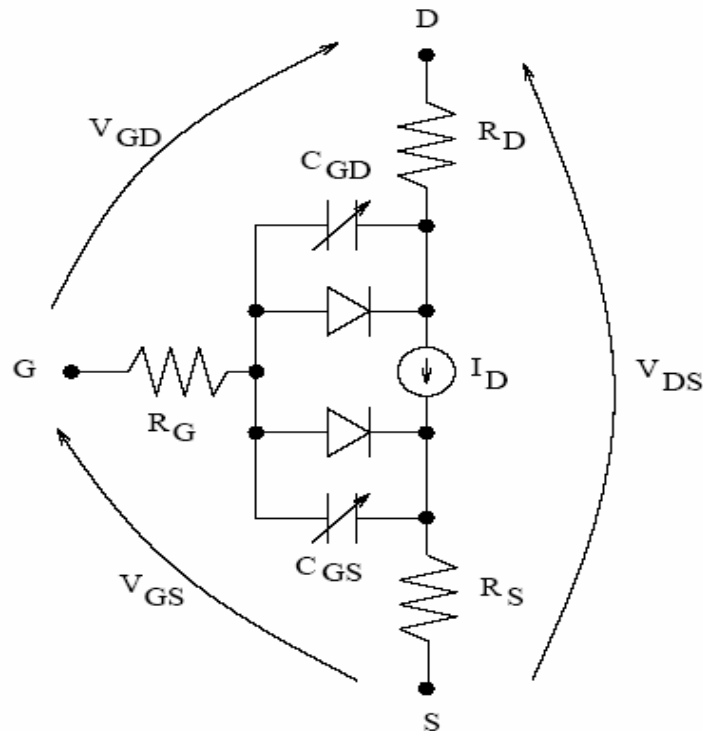
D-MESFET I-V characteristics:



The increase in drain current in saturation with V_{ds} is due to channel length modulation. The pinchoff point moves towards the source as V_{ds} increases, effectively shortening the gate length. The electric field becomes stronger in the region between the source and the pinch off point and the carrier velocity is increased.

MESFET Model

The Equivalent circuit model for a MESFET:



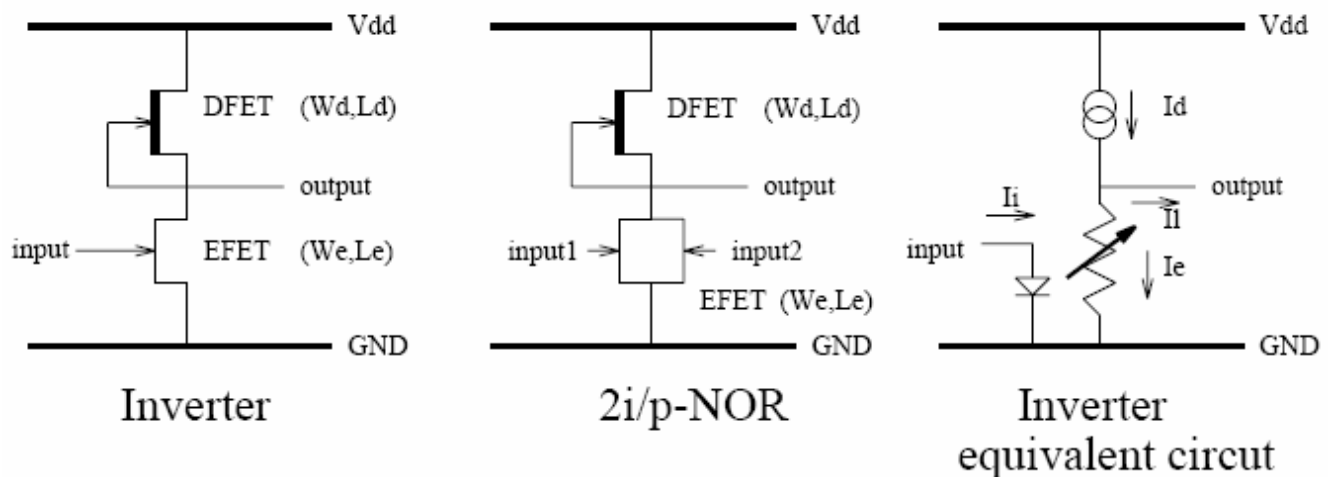
- C_{gd} and C_{gs} are non-linear gate-drain and gate-source diodes.
- Drain current, I_{DS} can be modelled using the Curtice equation:

$$I_{DS} = \begin{cases} 0 & V_{GS} - V_t \leq 0 \\ \beta (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) & V_{GS} - V_t > 0 \end{cases}$$

- The first term is cutoff, the second term represents the linear and saturation regions.
- λ is the channel length modulation factor and α is the saturation factor.

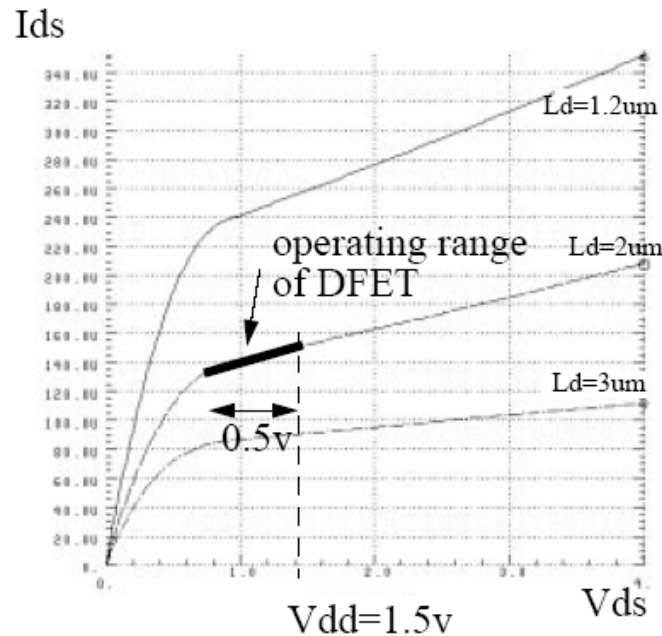
GaAs DCFL

The simplest logic family in GaAs is Direct Coupled FET Logic (DCFL) which is comparable to Silicon nMOS.



- DCFL is a *normally-off* class of logic and uses an enhancement mode MESFET (EFET) as a switch and a depletion mode MESFET (DFET) operating in saturation as a load.
- DCFL has the smallest power-delay product of the GaAs logic families. (70ps, 0.2mW)
- When cascaded, the high level output of the first gate is clamped to about 0.7V by the Schottky diode at the input of the second gate. In this sense the gate switches current from the EFET to the load.
- This limits the voltage swing of the gate and hence the noise margin to around 100mV.
- The pull down to pull up $(W_e.L_d/W_d.L_e \sim 10/1)$ MESFET ratio determines the noise margin, propagation delay and transition times.

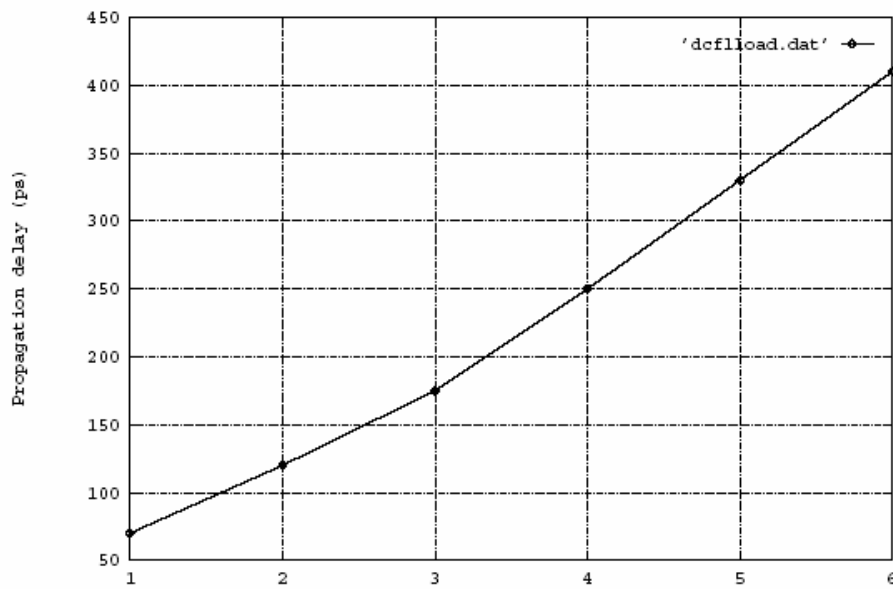
- DCFL produces a quieter power bus since the DFET operates in saturation as a current source.
- A relatively small change in current drawn from the supply in the high and low logic states also contributes to circuit stability.
- To achieve low power the current in the DFET must be made small, hence the gate width must be small and the length long.



e.g. For a DFET with a gate length of $L_d = 2\mu\text{m}$ and a $V_{dd} = 1.5\text{V}$ power supply, the current is $I_{DSS} = 0.15\text{mA}$, so the static power dissipation per gate is, $P_s = I_{DSS} \cdot V_{dd} = 0.225\text{mW}$

- Increasing the power supply voltage pushes the DFET further into saturation and makes the changes in supply current even smaller at the expense of power dissipation.
- Dynamic power dissipation is a small component of P_s , since each stage is inverting, the power dissipation is almost constant.

- A major drawback of DCFL is its poor load drive capability since the DFET is always on and the switching EFET must supply current to both pull the load down and also supply the load DFET. (Complementary logic classes drive the load with just one device while the other is cut off.)



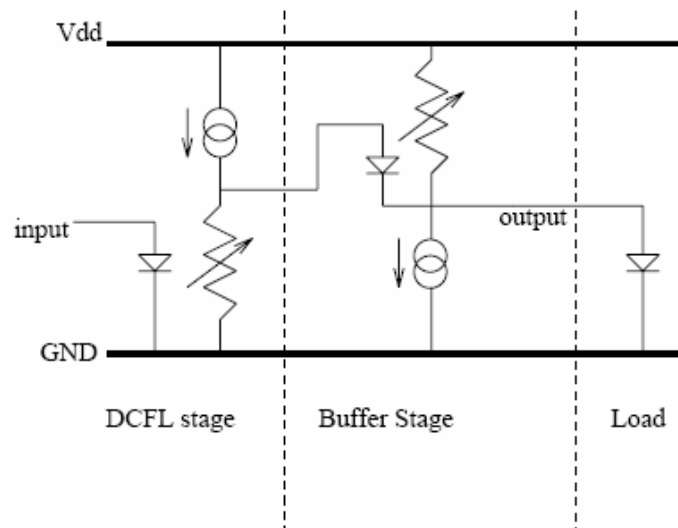
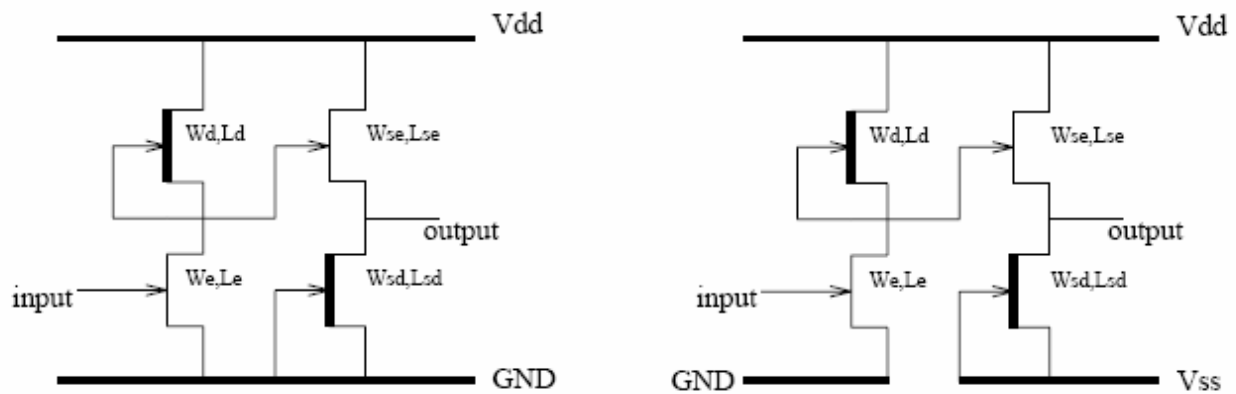
- A buffered logic should be used to drive these higher loads.

Exercises:

- Determination of pull-up to pull-down ratio:
- Determination of rise and fall times

GaAs ADCFL

- Source Follower DCFL (SDCFL) is a buffered logic class based on DCFL to improve the load drive capability, voltage swing and noise margin.



- The buffer is a source follower using an EFET as a pull-up and a DFET as a pull-down load.
- The output of the DCFL stage is clamped at two diode drops across the EFET in the source follower and across the input diode of the DCFL load. The voltage swing is improved over the DCFL class (internally it is around 1.3V).
- An extra negative supply rail may be used to isolate the buffer ground from the DCFL stage since it is noisier.

- SDCFL can have a fan-in of up to 5, where as DCFL is usually limited to 3.
- OR-AND-INVERT structures can be made such as $Z = \overline{(A+B)} \cdot \overline{C}$ by wire-or'ing the output of two SDCFL gates.