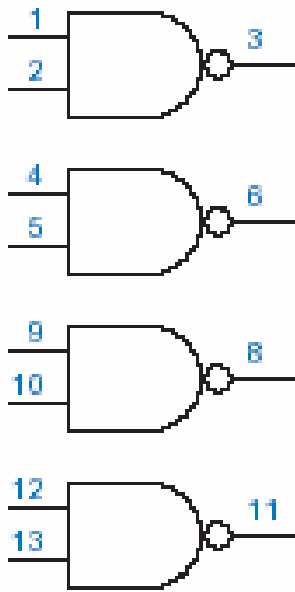
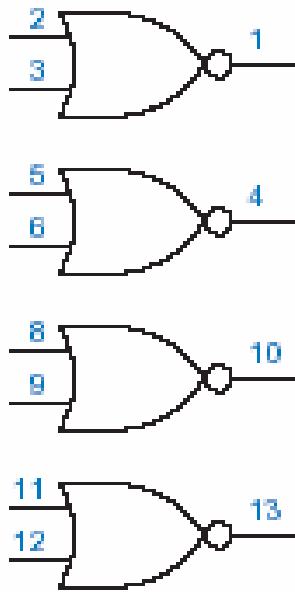


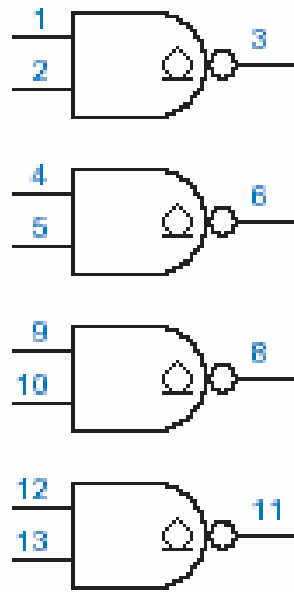
74x00



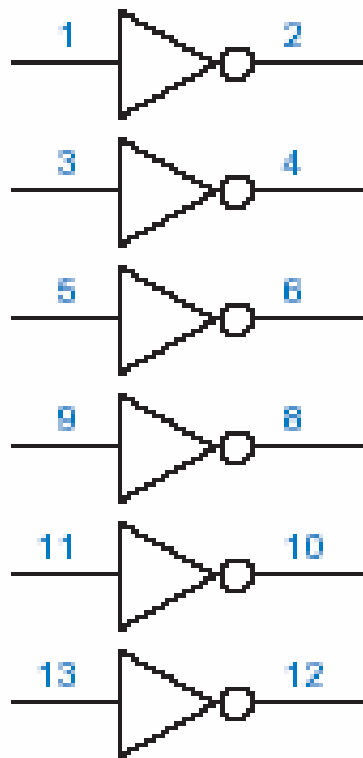
74x02



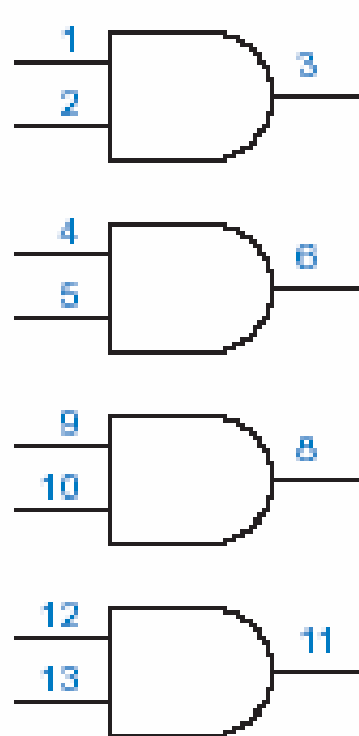
74x03



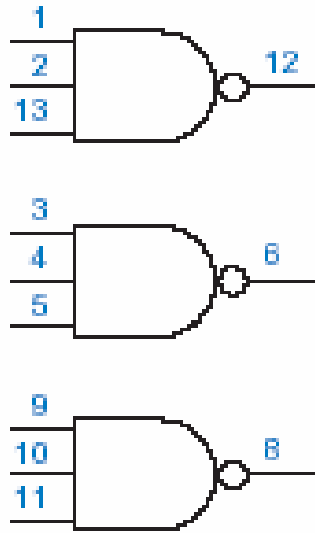
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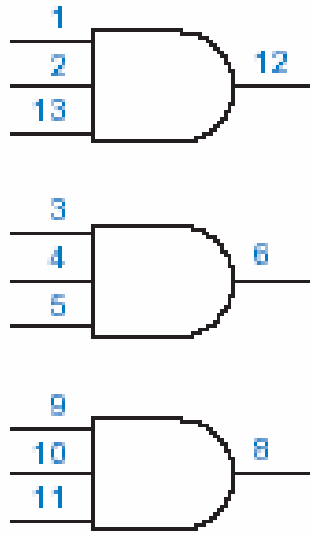
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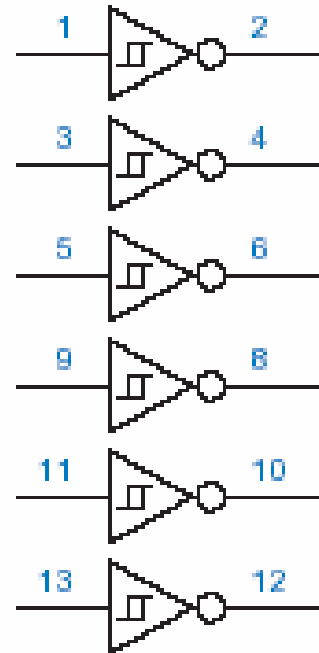
74x10



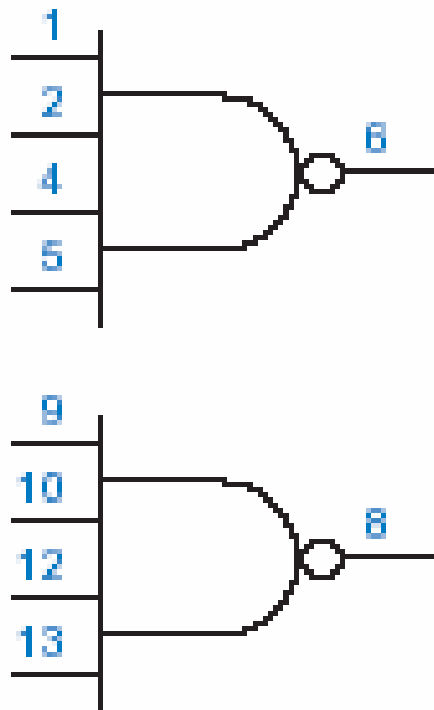
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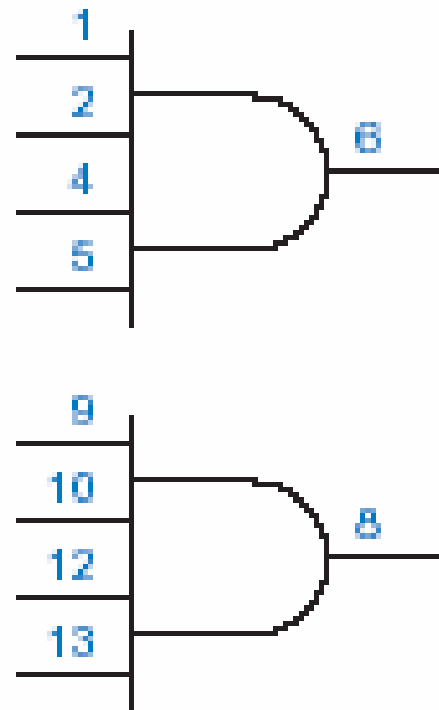
74x14



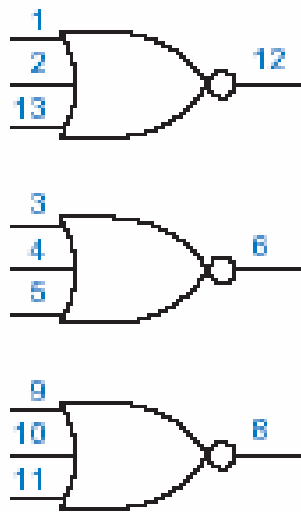
74x20



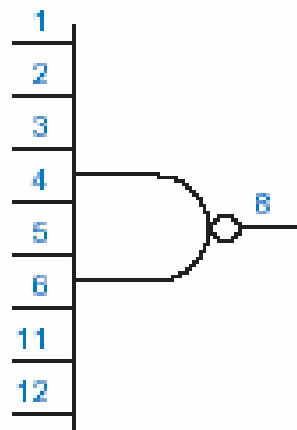
74x21



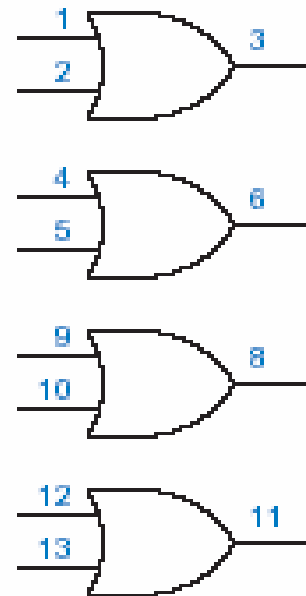
74x27



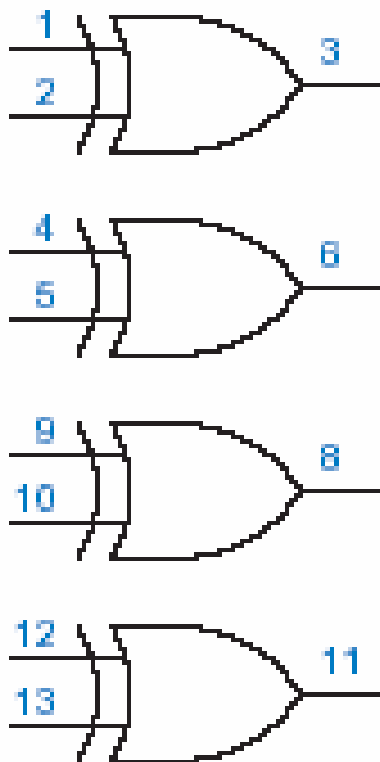
74x30



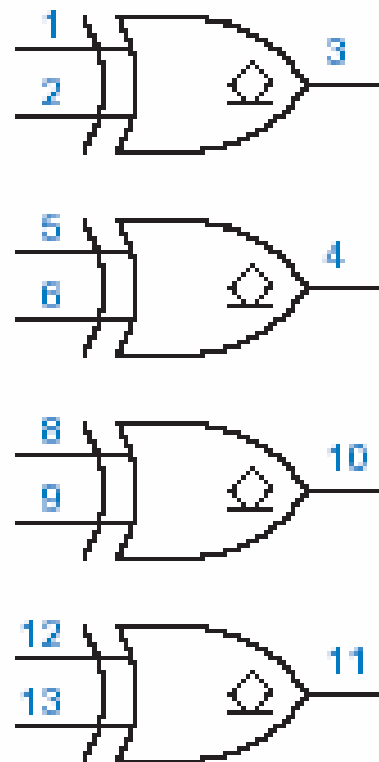
74x32



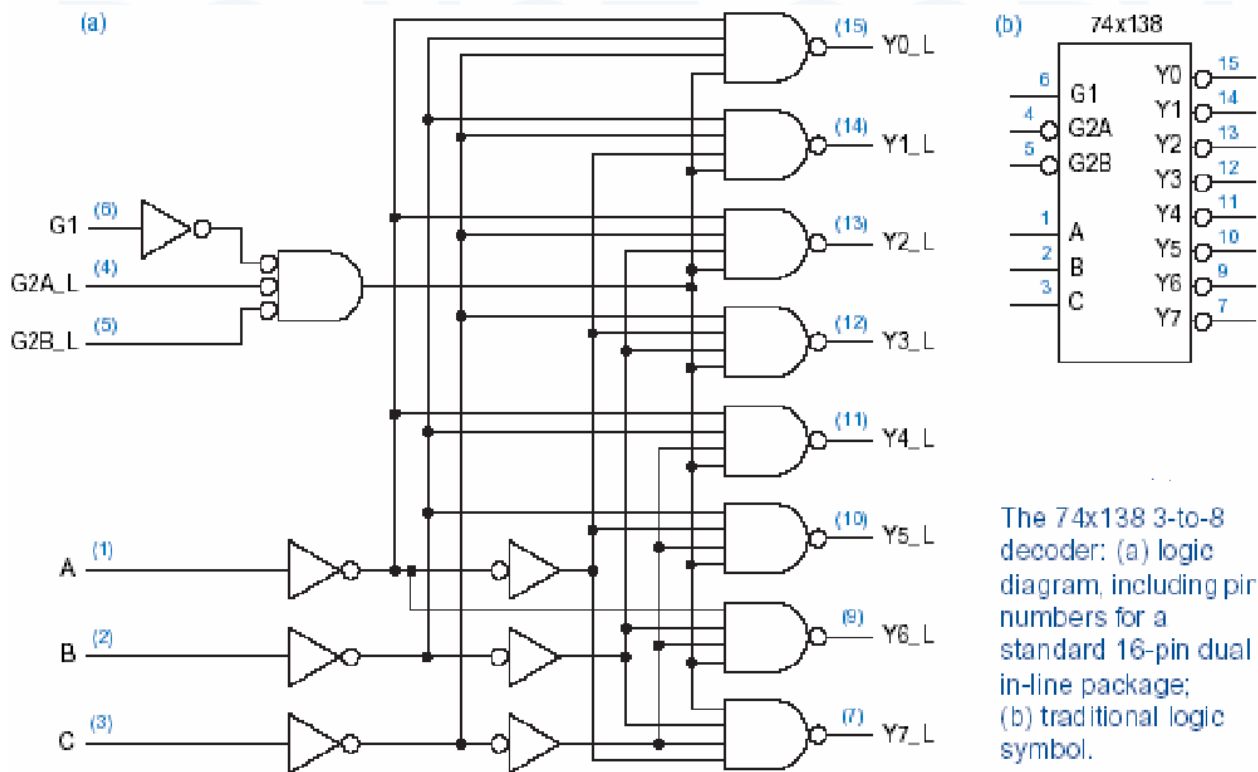
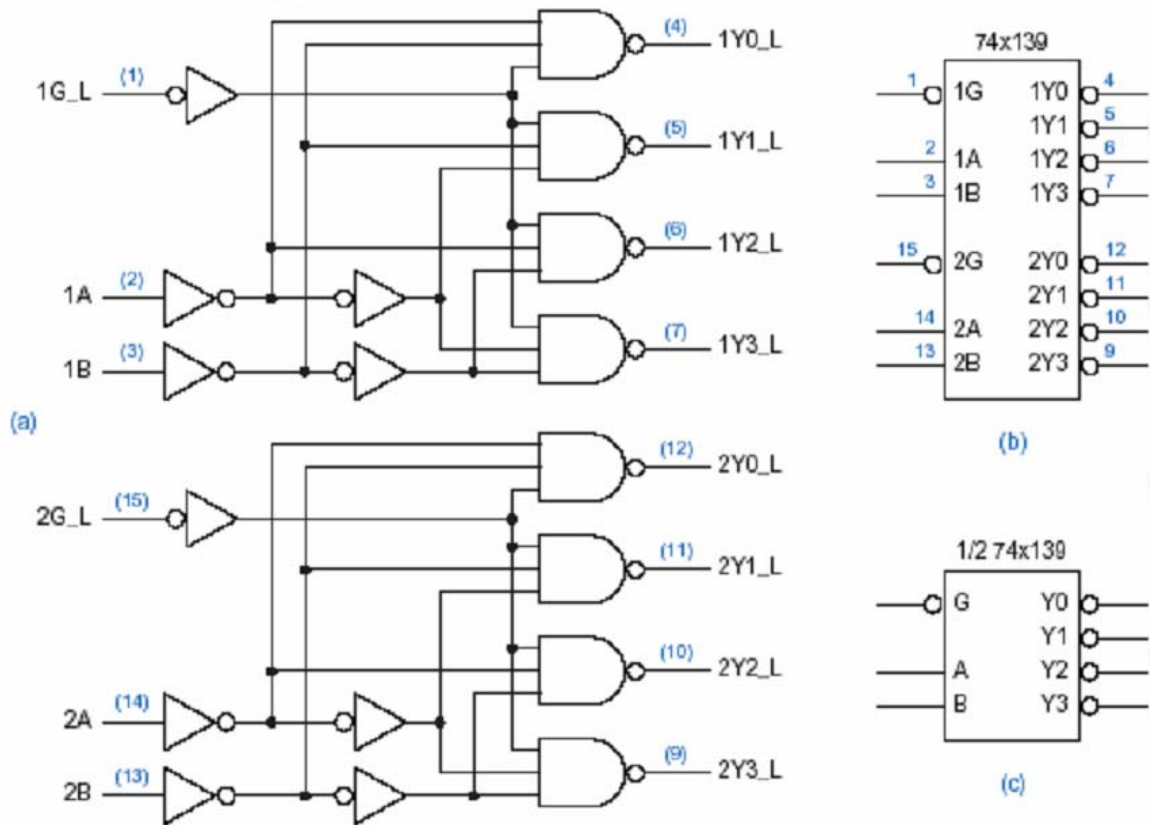
74x86



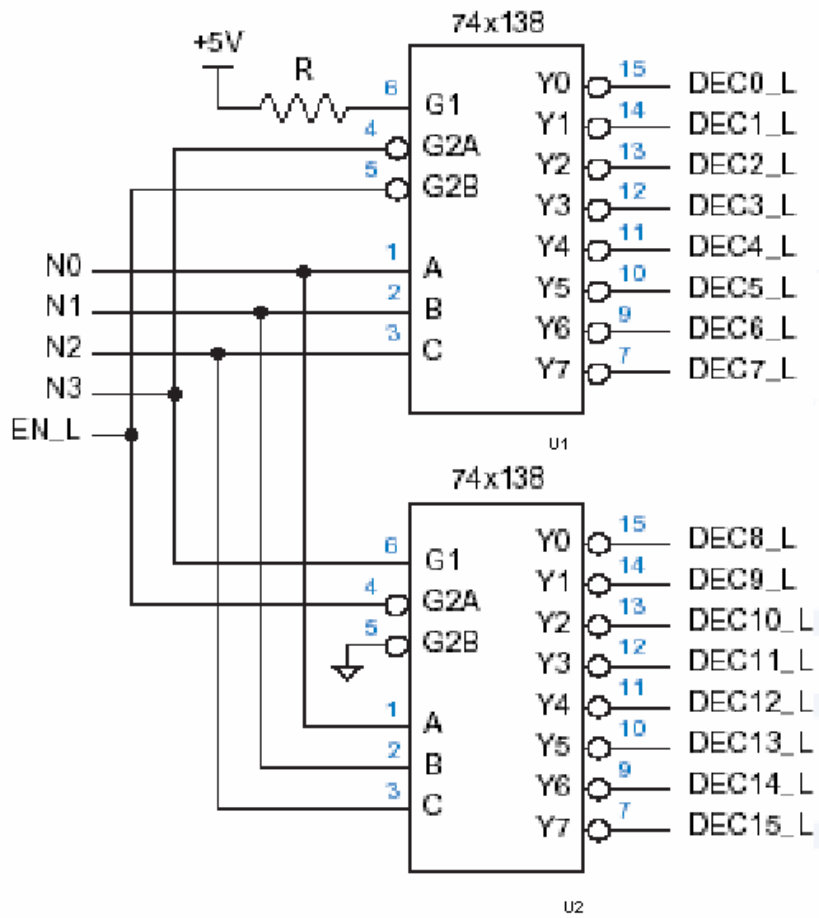
74x266



The 74x139 dual 2-to-4 decoder: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol; (c) logic symbol for one decoder.



The 74x138 3-to-8 decoder: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.



Design of a 4-to-16 decoder using 74x138s.

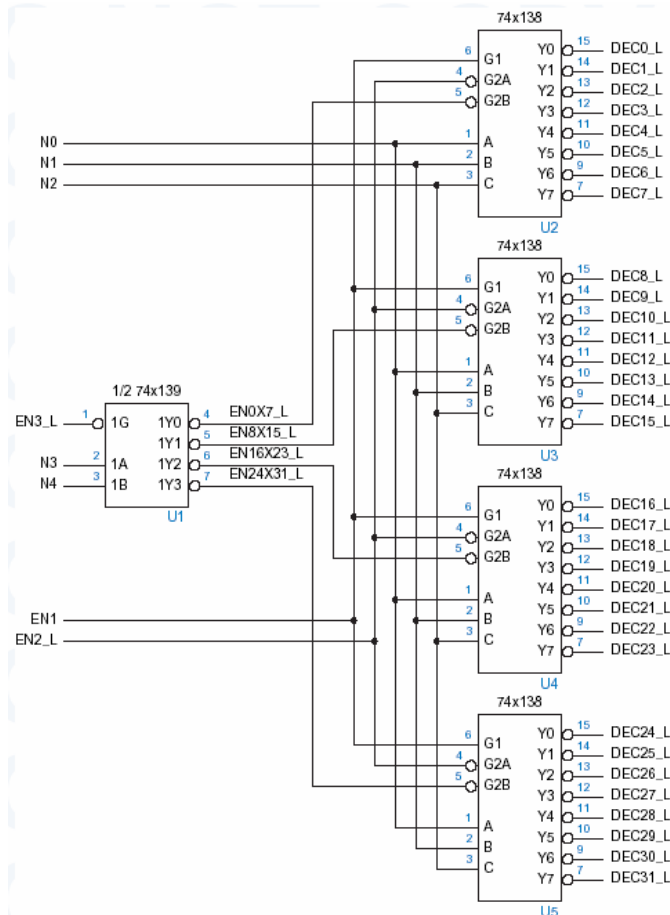


Figure 5-39 Design of a 5-to-32 decoder using 74x138s and a 74x139.